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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,517	04/19/2001	Nobuo Suzuki	107317-00028	8208

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EXAMINER	
DANIELS, ANTHONY J	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,517	SUZUKI ET AL.	
	Examiner	Art Unit	
	Anthony J. Daniels	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,8,10,11,15,16,19 and 20* is/are allowed.

6)☒ Claim(s) *1-6,9,13,14,17,18 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. The amendment, filed 2/18/2005, has been entered and made of record. Claims 1-24 are pending in the application.

2. Applicant's arguments to examiner's objection to the drawings, Remarks, p. 14, para. 7, have been considered and are persuasive. Accordingly, examiner's objection to the drawings has been withdrawn.

3. Applicant's amendment to the title of the invention has overcome examiner's objection.

Response to Arguments

4. Applicant's arguments filed 2/18/2005 have been fully considered but they are not persuasive. Examiner's arguments are set forth in the context of the standing rejections below.

Claim Rejections - 35 USC § 112

5. Claims 3,6,9,12 stand rejected and claims 21-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. *Applicant refers to the electronic shutter operation as sequentially draining charges by supplying a reset signal to a reset line from said reset row-shifter in claim 1. In claims 3,6,9, and 12, applicant claims that if a still image mode indication signal is received during an electronic shutter operation, an image signal readout operation is performed following the electronic shutter operation. Once the electronic shutter*

operation is finished, there are no charges in the photoelectric conversion elements to be readout. There is no utilization for this operation. ***Examiner concedes that "following said shutter operation" does not limit the image signal read operation to be performed immediately following the electronic shutter operation, but according to the claim language "and thereafter said flashing device signal is made", the flashing device operation signal cannot be made until an image signal read operation has occurred. Since the flashing operation occurs during an exposure time implies that an exposure does not exist between the electronic shutter operation and flashing operation. Therefore, the claim language sets forth that an image signal read operation occurs when no charge is accumulated in the photodiodes.***

As to claims 21-24, claims 21-24 are rejected as being dependent upon the rejected claims 3,6,9,12, respectively. Examiner suggests that the language "and after a lapse in exposure time", if incorporated into claims 3,6,9,12 would overcome examiner's rejection.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1,2,4,5,13,14,17,18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Juen (US # 6,542,194) in view of Yamagishi (US # 6,710,808).

As to claim 1, Juen teaches an electronic camera (see Figure 4) comprising: a MOS type solid-state image pickup device (see Figure 4, imaging element "45"; Col. 13, Lines 41-44) comprising (i) a semiconductor substrate *{It is well known that MOS type image sensors are built upon a semiconductor substrate.}*, (ii) a number of photoelectric conversion elements (see Figure

8, PD 11,12, 21,22, etc.) formed in one surface of said semiconductor substrate in a matrix shape along a plurality of rows and columns (see Figure 8), (iii) a switching circuit provided for each photoelectric conversion element and electrically connected to an corresponding photoelectric conversion element (see Figure 8, transistors circuit consisting of "QTij","QAij", and "QRSTij") each switching circuit controlling generation of an output signal representative of charges accumulated in said corresponding photoelectric conversion element and drainage of said charges (see Col. 9, Lines 25-32; Col. 14, Lines 5,6), (iv) a row selection signal line disposed for each photoelectric conversion element row (see Figure 8, line corresponding to signal "ΦTR1") and electrically connected to corresponding switching circuits (see Figure 8), each row selection signal line being supplied with a row selection signal for controlling generation of said output signal (see Col. 10, Lines 62-65), (v) a plurality of output signal lines each of which is corresponded to at least one pixel column (see Figure 8, line "LV1,2,3,...) and on each of which said output signal is generated (see Col. 11, Lines 21-29), vi) a reset signal line disposed for each photoelectric conversion element row and electrically connected to corresponding switching circuits (see Figure 8, line connected to the drain of transistor "QRSTij"), each reset signal line being supplied with a reset signal for controlling drainage of said charges (see Figure 8, "ΦRDi"; Col. 10, Lines 62-65), (vii) a readout row-shifter (see Figure 8, signal reading scanning register "62") for sequentially supplying said row selection signal to each row selection signal line (see Col. 11, Lines 58-64), (viii) a reset row-shifter (see Figure 8, reset scanning register "63") for sequentially supplying said reset signal to each reset signal line (see Col. 11, Lines 65-67, Col. 12, Lines 1-6), and (ix) an output device electrically connected to each output signal line (see Figure 8, circuit consisting of transistor "QTCsi", capacitor "CTsi") for sequentially generating

and outputting image signals representative of said output signals (see Col. 11, Lines 24-27), an image signal processor for generating moving image data or still-image data based on said image signals output from said MOS type solid-state image pickup device (see Figure 4, signal processor "48", Col. 3, Lines 16-19; image display "49"), a still image indication signal generator for generating a still image indication signal for indicating image pickup of a still image (see Col. 7, Lines 61-63), a moving image mode controller (see Figure 4, CPU "52") being connected to said MOS type solid-state image pickup device for continually controlling operation of said MOS type solid-state image pickup device (see Col. 7, Lines 45-55), said moving image mode controller makes said MOS type solid-state image pickup device repeat (a) an image signal read operation of sequentially supplying said row selection signal from the readout row-shifter to a plurality of predetermined row selection signal lines for sequentially generating said output signals on each output signal line (see Col. 10, Lines 50-65) and (b) an electronic shutter operation of sequentially supplying said reset signal from the reset row-shifter to said reset signal lines corresponding to at least said rows to be subjected to said image signal read operation for sequentially draining said charges accumulated in the photoelectric conversion elements (see Col. 5, Lines 35-37), and a correcting still image mode controller being connected to said MOS type solid-state image pickup device (see Figure 4, CPU "52") for controlling operation of said MOS type solid-state image pickup device (see Col. 7, Lines 45-55) in place of said moving image mode controller when said still image indication signal is made (see Col. 7, Lines 61-63), an exposure time of each photoelectric conversion element is set equal to or shorter than a time duration including an issuance time of a flashing device operation signal and necessary for performing two image signal read operations before and after one electronic shutter

operation (see Figure 2A, exposure time "Tex", *{As seen from the timing diagram, one signal reading period is longer than the exposure time, let alone two, and any other time duration signal, namely a flashing device operation signal combined with the time of two signal readout operations will be longer than the exposure time.}*, and after a lapse of said exposure time, said correcting still image mode controller makes said MOS type solid-state image pickup device perform an image signal read operation of sequentially supplying said row selection signal from the readout row-shifter to each row selection signal line for sequentially generating said output signals on each output signal line (see Figure 2A, *{The signal readout is performed after the exposure time, Tex.}*). The claim differs from Juen in that it requires that a flashing device for emitting a flash in reception to a predetermined signal be included in the electronic camera, and that the signal is made in a state where the readout row shifter and the reset row shifter are not operated.

In the same field of endeavor, Yamagishi teaches an electronic camera (see Figure 1) which contains a flashing device for emitting a flash (see Figure 1, electronic flash portion "48", Col. 5, Lines 14-16) in response to the reception of a predetermined signal (see Figure 1, Col. 7, Line 4, *{Signal comes from the flash setup button, goes to the system control circuit and outputs a signal to the electronic flash portion.}*), and that the signal is made at a state where the readout row shifter and the reset row shifter are not operated (see Figure 7 and 8, *{The flash signal (S307) is made at a point when the CCD, or CMOS (see Col. 3, Line 51) has already been cleared (S303) and the signal readout hasn't happened yet (S315).}*). ***In regard to the arguments from Remarks, p. 17, para. 2, the examiner respectfully disagrees. Applicant correctly points out that Juen teaches that the rows are reset, exposed, and read sequentially,***

and further claims that "...once the reset scanning begins during still image shooting in Juen, the entire array is not simultaneously exposed. Emitting the flash of Yamagishi after resetting and before reading the pixels during still image shooting in Juen (i.e., at any time during still image shooting in Juen) cannot occur at a period when the readout row-shifter and reset row-shifter are not operated." There is a period when the row is reset, a period when the row is exposed, and a period when the signals are read. The period when the row is exposed, ie. exposure time, is a definitive period when the readout and reset operations are not performed. It is well-known that a flash occurs during an exposure time, and for as long as an exposure time. In regard to the arguments from Remarks, p. 17, para. 3, it respectfully submitted that the Yamagishi teaches the use of flashing on either a CCD or CMOS device (Col. 3, Lines 46-49). In regard to the arguments from Remarks, p. 18, para. 1, it is respectfully submitted that Juen teaches a point in the exposure during which neither the reset operation nor the read operation are occurring (Figure 2A, period after the reset ends (dotted line) to when the read starts (pixel signal reading position 6)). In light of the teaching of Yamagishi, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electronic camera of Juen to include a flashing device where a flash is emitted in response to the reception of a predetermined signal and the predetermined signal is made at a point where the readout row shifter and the reset row shifter are not operated. Such a modification would allow for an object to be captured to be more illuminated, so an image of said object can be faithfully presented, and having the readout row shifter and the reset row shifter inoperable during the flash signal, allows for constant framing intervals of image sensing (see Yamagishi, Col. 2, Lines 53-55) that prevent sensing images of uneven quality.

As to claim **2**, Juen, as modified by Yamagishi, teaches an electronic camera according to claim 1 (see 103(a) rejection above), wherein the image signal read operation by said moving image mode controller and the image signal read operation by said correcting still image mode controller include (i) operation of sequentially supplying said row selection signal from the readout row-shifter to a plurality of predetermined row selection signal lines for sequentially generating said output signals on each output signal line in the unit of a photoelectric conversion element row (see Juen, Col. 10, Lines 50-65) and (ii) operation of sequentially draining said charges accumulated in each photoelectric conversion element from which said output signal was generated, in the unit of a photoelectric conversion element row (see Juen, Col. 10, Lines 65-67, Col. 11, Lines 1-6).

As to claim **4**, Juen, as modified by Yamagishi, teaches an electronic camera according to claim 1 (see 103(a) rejection above), further comprising: a non-correcting still image mode controller being connected to said MOS type solid-state image pickup device (see Figure 4, CPU "52") for controlling operation of said MOS type solid-state image pickup device (see Col. 7, Lines 45-55) in place of said moving image mode controller when said still image signal is made, wherein without making said flashing device operation signal (see Figure 7, "S307"), said non-correcting still image mode controller makes said MOS type solid-state image pickup device perform an image signal read operation of sequentially supplying said row selection signal from the readout row-shifter to each row selection signal line for sequentially generating said output signals on each output signal line (see claim 2 rejection above; see Yamagishi, Figure 8, "S315"); and still image mode designating device for specifying beforehand a still image mode controller to be operated when said still image indication signal is made (see Col. 7, Lines 61-63,

{Designating device is the button.}).

As to claim **5**, the limitations in claim 5 can be found in claim 2. Therefore, claim 5 is analyzed and rejected as previously discussed with respect to claim 2.

As to claim **13**, Juen, as modified by Yamagishi, teaches an electronic camera according to claim 1 (see 103(a) rejection above), further comprising: an auto iris for adjusting an amount of light incident upon said MOS type solid-state image pickup device (see Juen, Figure 1, mechanical focal plane shutter "1"), wherein said correcting still image mode controller in operation further performs an exposure amount adjustment operation of adjusting said auto iris to reduce a difference between exposure amounts to be caused by a difference between an exposure time under a control of said correcting still image mode controller and an exposure time under a control of said moving image mode controller (see Juen, Col. 9, Lines 11-24).

As to claim **14**, the limitations in claim 14 can be found in claim 13. Therefore, claim 14 is analyzed and rejected as previously discussed with respect to claim 13.

As to claim **17**, Yamagishi teaches a digital output device that receives said analog signals, converts the analog signals into digital signals, and outputs the digital signals (see Figure 1, A/D Converter "16").

As to claim **18**, the limitations of claim 18 can be found in claim 17. Therefore claim 18 is analyzed and rejected as previously discussed with respect to claim 17.

Allowable Subject Matter

7. Claims 7,8,10,11,15,16,19,20 allowed.

The reasons for allowance can be found in the prior Office action.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AD
6/16/2005

NGOC-YEN VU
PRIMARY EXAMINER